FIGURE 1

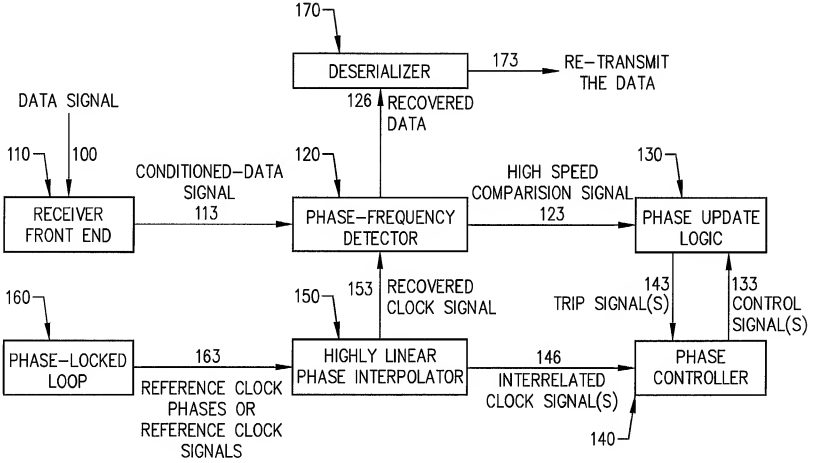


FIGURE 2

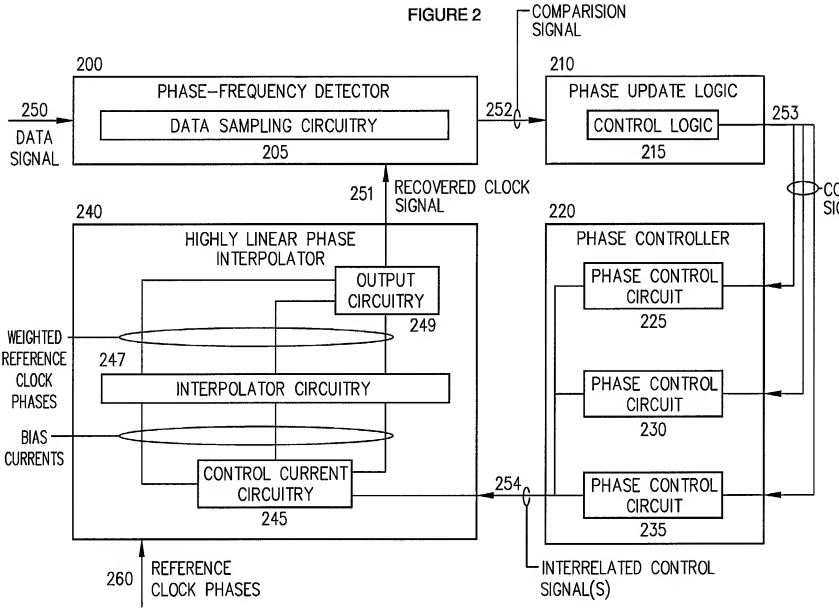


FIGURE 3A

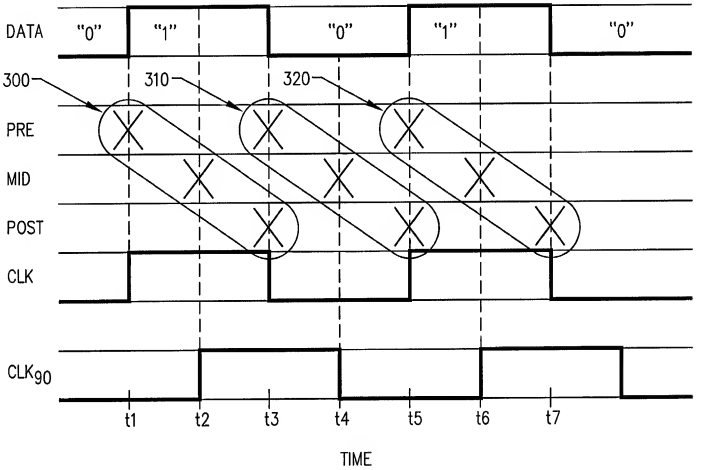


FIGURE 3B

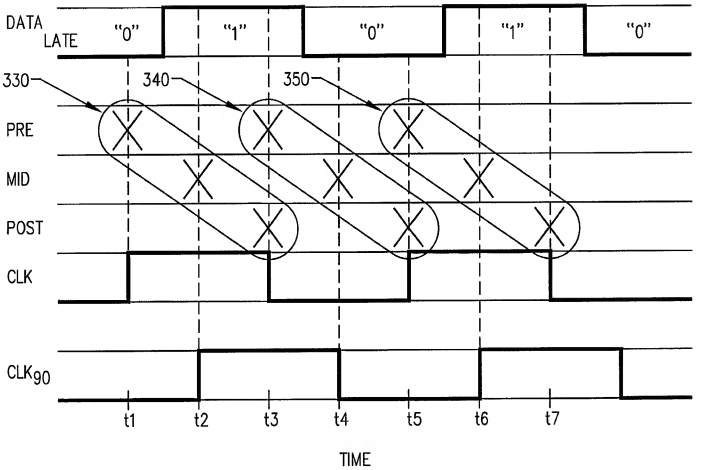


FIGURE 3C

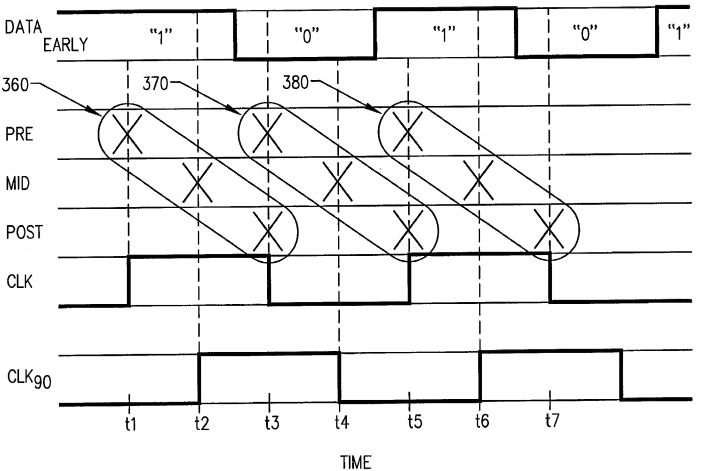


FIGURE 4

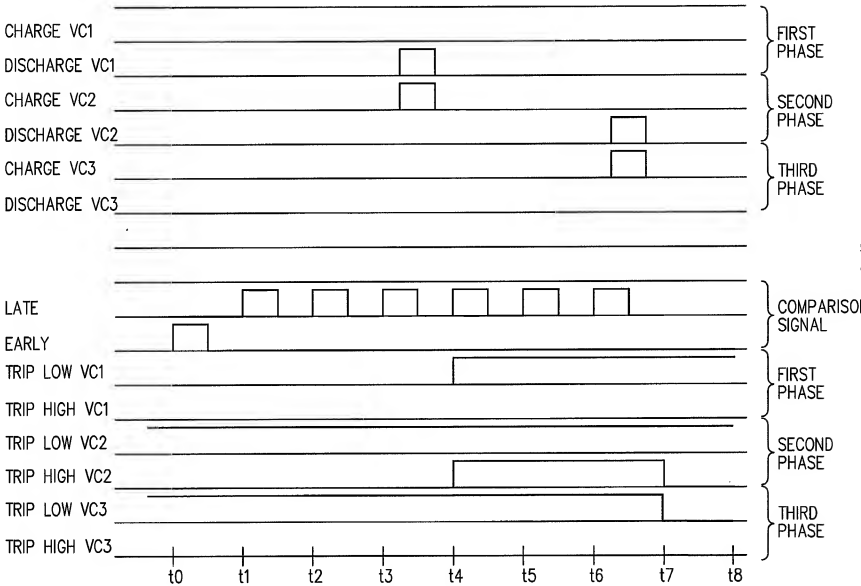

CHARGE VC1
DISCHARGE VC1
CHARGE VC2
DISCHARGE VC2
CHARGE VC3
DISCHARGE VC3
FIRST PHASE
SECOND PHASE
THIRD PHASE
LATE
EARLY
COMPARISON SIGNAL
TRIP LOW VC1
TRIP HIGH VC1
TRIP LOW VC2
TRIP HIGH VC2
TRIP LOW VC3
TRIP HIGH VC3
FIRST PHASE
SECOND PHASE
THIRD PHASE
t0
t1
t2
t3
t4
t5
t6
t7
t8

FIGURE 5

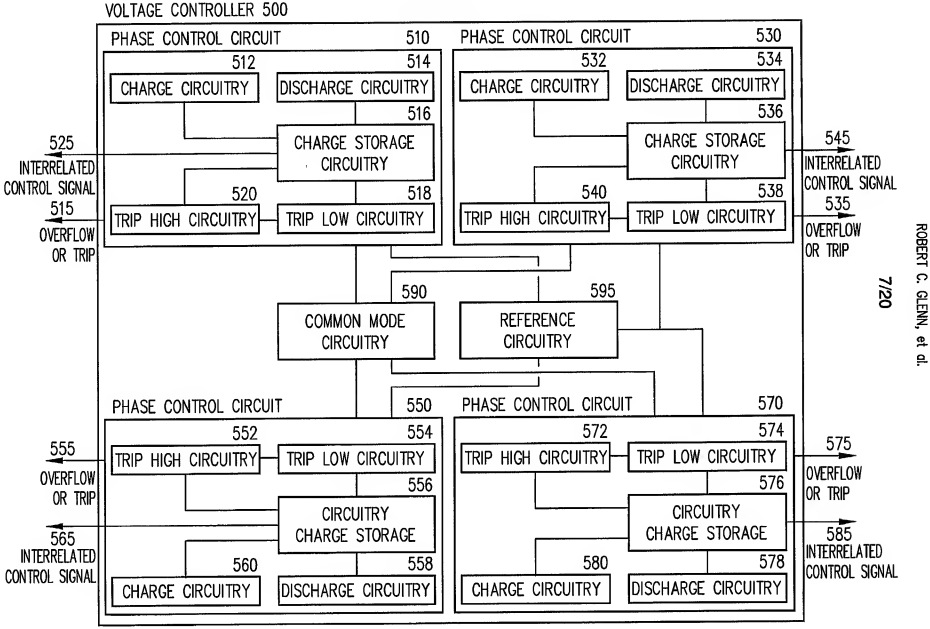

VOLTAGE CONTROLLER 500
PHASE CONTROL CIRCUIT
510
512
CHARGE CIRCUITRY
514
DISCHARGE CIRCUITRY
516
CHARGE STORAGE CIRCUITRY
520
TRIP HIGH CIRCUITRY
518
TRIP LOW CIRCUITRY
525
INTERRELATED CONTROL SIGNAL
515
OVERFLOW OR TRIP
PHASE CONTROL CIRCUIT
530
532
CHARGE CIRCUITRY
534
DISCHARGE CIRCUITRY
536
CHARGE STORAGE CIRCUITRY
540
TRIP HIGH CIRCUITRY
538
TRIP LOW CIRCUITRY
545
INTERRELATED CONTROL SIGNAL
535
OVERFLOW OR TRIP
590
COMMON MODE CIRCUITRY
595
REFERENCE CIRCUITRY
PHASE CONTROL CIRCUIT
550
552
TRIP HIGH CIRCUITRY
554
TRIP LOW CIRCUITRY
556
CIRCUITRY CHARGE STORAGE
560
CHARGE CIRCUITRY
558
DISCHARGE CIRCUITRY
555
OVERFLOW OR TRIP
565
INTERRELATED CONTROL SIGNAL
PHASE CONTROL CIRCUIT
570
572
TRIP HIGH CIRCUITRY
574
TRIP LOW CIRCUITRY
576
CIRCUITRY CHARGE STORAGE
580
CHARGE CIRCUITRY
578
DISCHARGE CIRCUITRY
575
OVERFLOW OR TRIP
585
INTERRELATED CONTROL SIGNAL

FIGURE 6

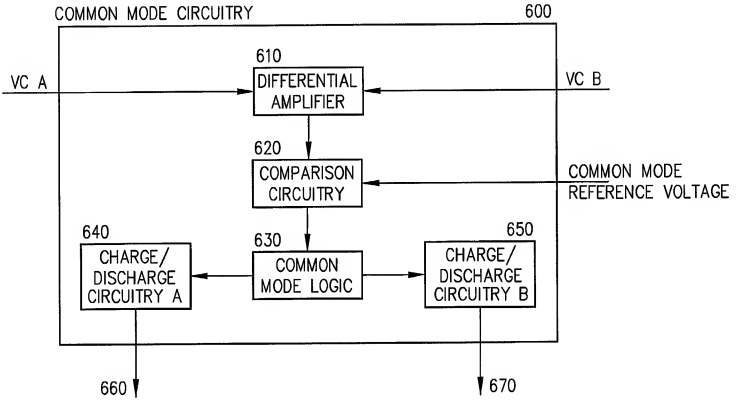

COMMON MODE CIRCUITRY
600
610
DIFFERENTIAL AMPLIFIER
VC A
VC B
620
COMPARISON CIRCUITRY
COMMON MODE REFERENCE VOLTAGE
640
CHARGE/ DISCHARGE CIRCUITRY A
630
COMMON MODE LOGIC
650
CHARGE/ DISCHARGE CIRCUITRY B
660
670

FIGURE 7

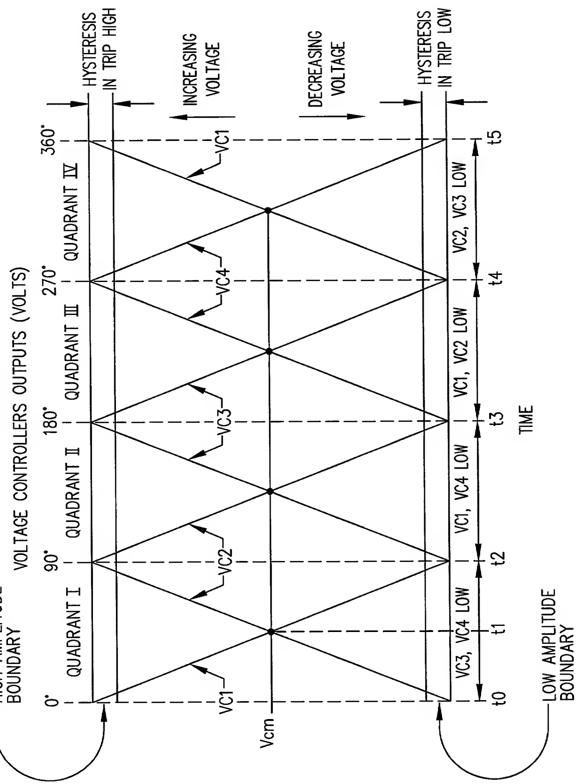


FIGURE 8

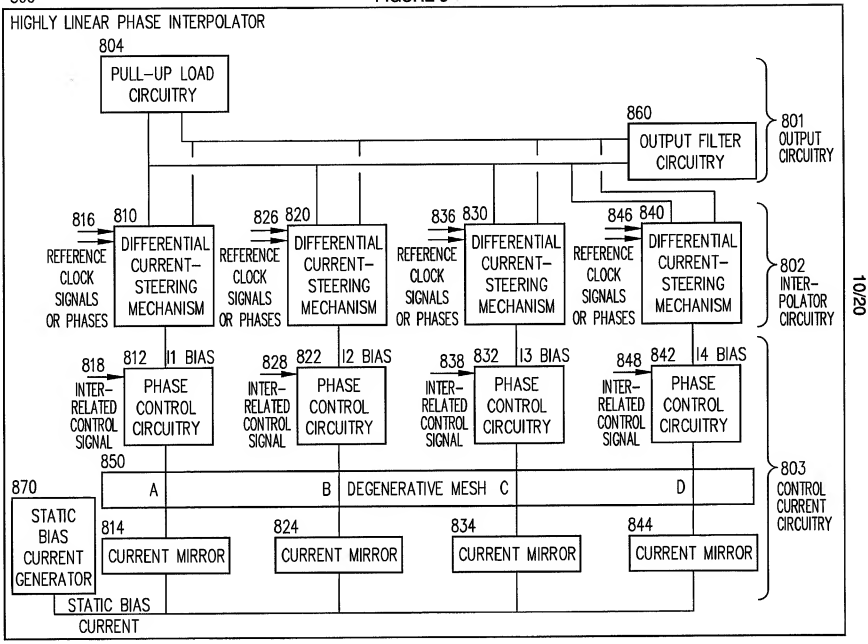
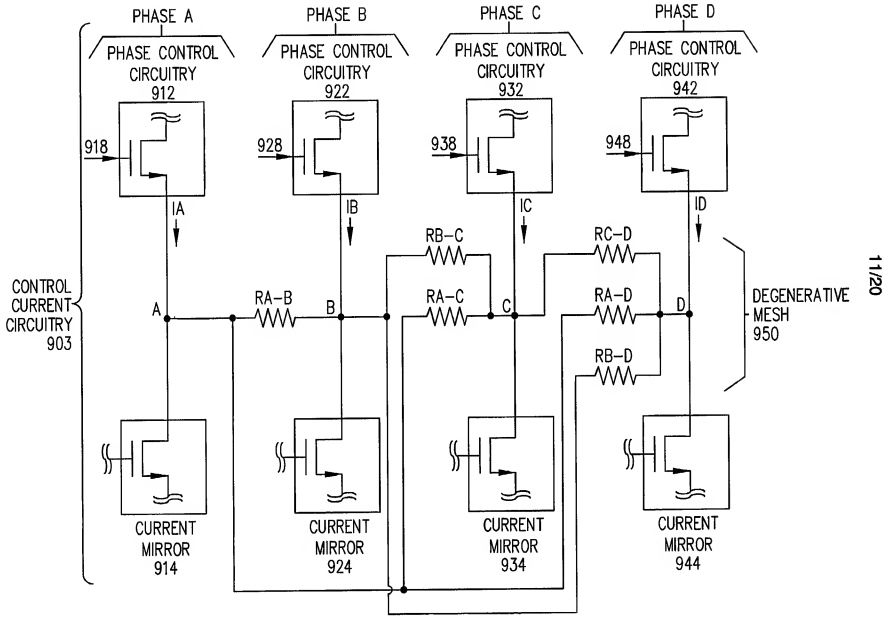

800
HIGHLY LINEAR PHASE INTERPOLATOR
804
PULL-UP LOAD CIRCUITRY
860
OUTPUT FILTER CIRCUITRY
801 OUTPUT CIRCUITRY
816
810
DIFFERENTIAL CURRENT-STEERING MECHANISM
REFERENCE CLOCK SIGNALS OR PHASES
826
820
836
830
846
840
802 INTER-POLATOR CIRCUITRY
818
812
I1 BIAS
PHASE CONTROL CIRCUITRY
INTER-RELATED CONTROL SIGNAL
828
822
I2 BIAS
838
832
I3 BIAS
848
842
I4 BIAS
850
870
A
B
DEGENERATIVE MESH
C
D
803 CONTROL CURRENT CIRCUITRY
STATIC BIAS CURRENT GENERATOR
814
824
834
844
CURRENT MIRROR
STATIC BIAS CURRENT

FIGURE 9


PHASE A
PHASE B
PHASE C
PHASE D
PHASE CONTROL CIRCUITRY 912
PHASE CONTROL CIRCUITRY 922
PHASE CONTROL CIRCUITRY 932
PHASE CONTROL CIRCUITRY 942
918
928
938
948
IA
IB
IC
ID
RB-C
RC-D
RA-B
RA-C
RA-D
RB-D
A
B
C
D
CONTROL CURRENT CIRCUITRY 903
DEGENERATIVE MESH 950
CURRENT MIRROR 914
CURRENT MIRROR 924
CURRENT MIRROR 934
CURRENT MIRROR 944

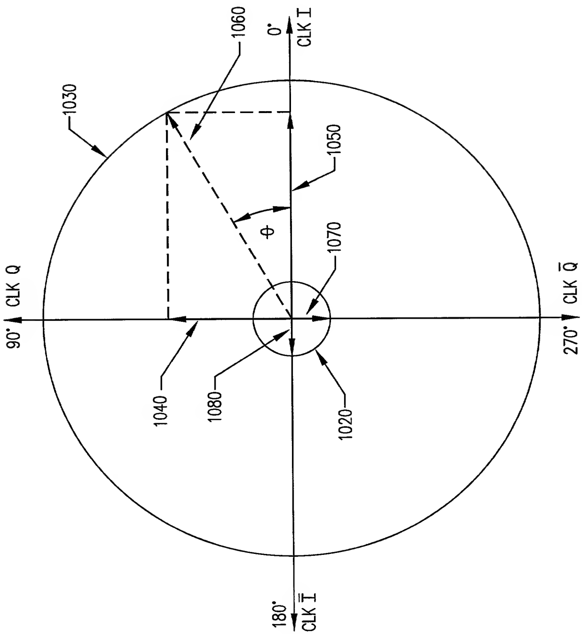
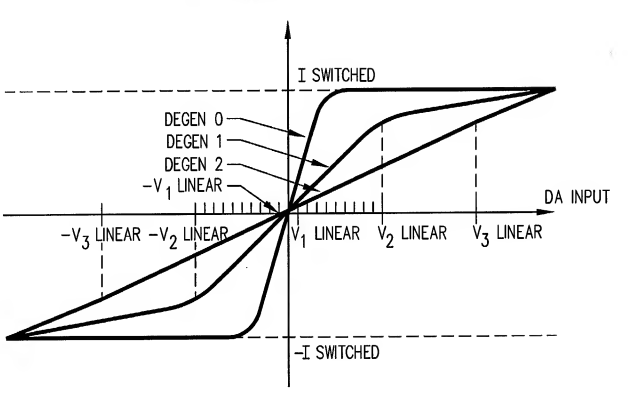

1060
0°
CLK I
1030
1050
Φ
1070
90°
CLK Q
1040
1080
1020
270°
CLK $\bar{Q}$
180°
CLK $\bar{I}$

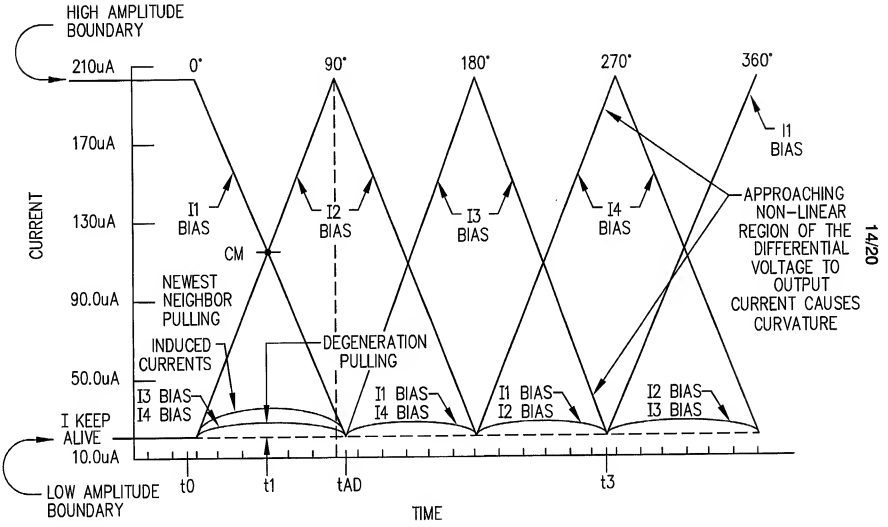
FIGURE 10

FIGURE 11



PSEUDO–DIFFERENTIAL AMPLIFIER SWING RANGE BASED ON DEGENERATION

FIGURE 12



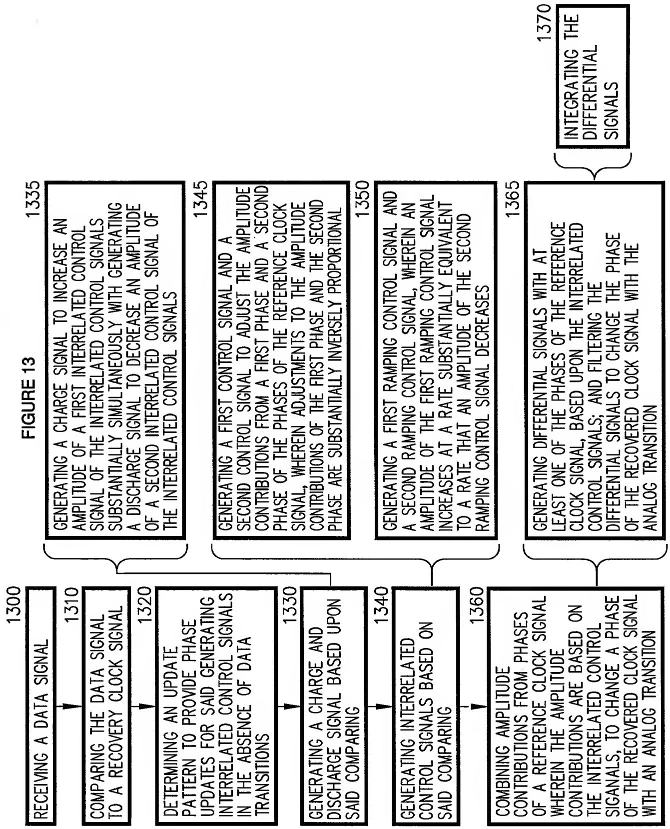

1300
RECEIVING A DATA SIGNAL
1310
COMPARING THE DATA SIGNAL TO A RECOVERY CLOCK SIGNAL
1320
DETERMINING AN UPDATE PATTERN TO PROVIDE PHASE UPDATES FOR SAID GENERATING INTERRELATED CONTROL SIGNALS IN THE ABSENCE OF DATA TRANSITIONS
1330
GENERATING A CHARGE AND DISCHARGE SIGNAL BASED UPON SAID COMPARING
1340
GENERATING INTERRELATED CONTROL SIGNALS BASED ON SAID COMPARING
1360
COMBINING AMPLITUDE CONTRIBUTIONS FROM PHASES OF A REFERENCE CLOCK SIGNAL WHEREIN THE AMPLITUDE CONTRIBUTIONS ARE BASED ON THE INTERRELATED CONTROL SIGANALS, TO CHANGE A PHASE OF THE RECOVERED CLOCK SIGNAL WITH AN ANALOG TRANSITION
1335
GENERATING A CHARGE SIGNAL TO INCREASE AN AMPLITUDE OF A FIRST INTERRELATED CONTROL SIGNAL OF THE INTERRELATED CONTROL SIGNALS SUBSTANTIALLY SIMULTANEOUSLY WITH GENERATING A DISCHARGE SIGNAL TO DECREASE AN AMPLITUDE OF A SECOND INTERRELATED CONTROL SIGNAL OF THE INTERRELATED CONTROL SIGNALS
1345
GENERATING A FIRST CONTROL SIGNAL AND A SECOND CONTROL SIGNAL TO ADJUST THE AMPLITUDE CONTRIBUTIONS FROM A FIRST PHASE AND A SECOND PHASE OF THE PHASES OF THE REFERENCE CLOCK SIGNAL, WHEREIN ADJUSTMENTS TO THE AMPLITUDE CONTRIBUTIONS OF THE FIRST PHASE AND THE SECOND PHASE ARE SUBSTANTIALLY INVERSELY PROPORTIONAL
1350
GENERATING A FIRST RAMPING CONTROL SIGNAL AND A SECOND RAMPING CONTROL SIGNAL, WHEREIN AN AMPLITUDE OF THE FIRST RAMPING CONTROL SIGNAL INCREASES AT A RATE SUBSTANTIALLY EQUIVALENT TO A RATE THAT AN AMPLITUDE OF THE SECOND RAMPING CONTROL SIGNAL DECREASES
1365
GENERATING DIFFERENTIAL SIGNALS WITH AT LEAST ONE OF THE PHASES OF THE REFERENCE CLOCK SIGNAL, BASED UPON THE INTERRELATED CONTROL SIGNALS; AND FILTERING THE DIFFERENTIAL SIGNALS TO CHANGE THE PHASE OF THE RECOVERED CLOCK SIGNAL WITH THE ANALOG TRANSITION
1370
INTEGRATING THE DIFFERENTIAL SIGNALS

FIGURE 13

FIGURE 14

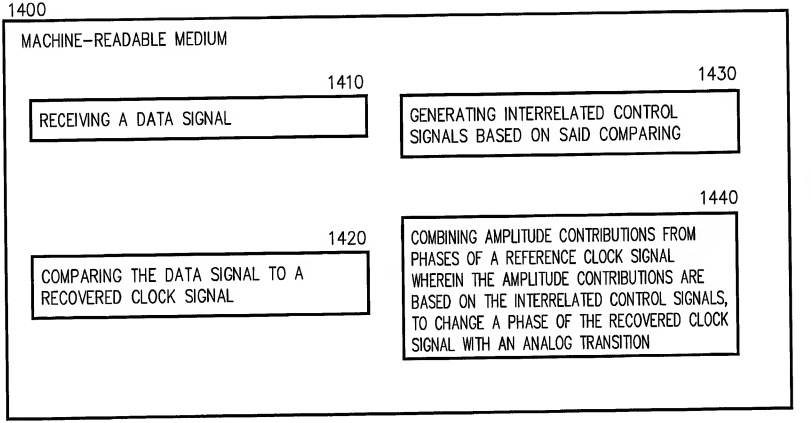


FIGURE 15

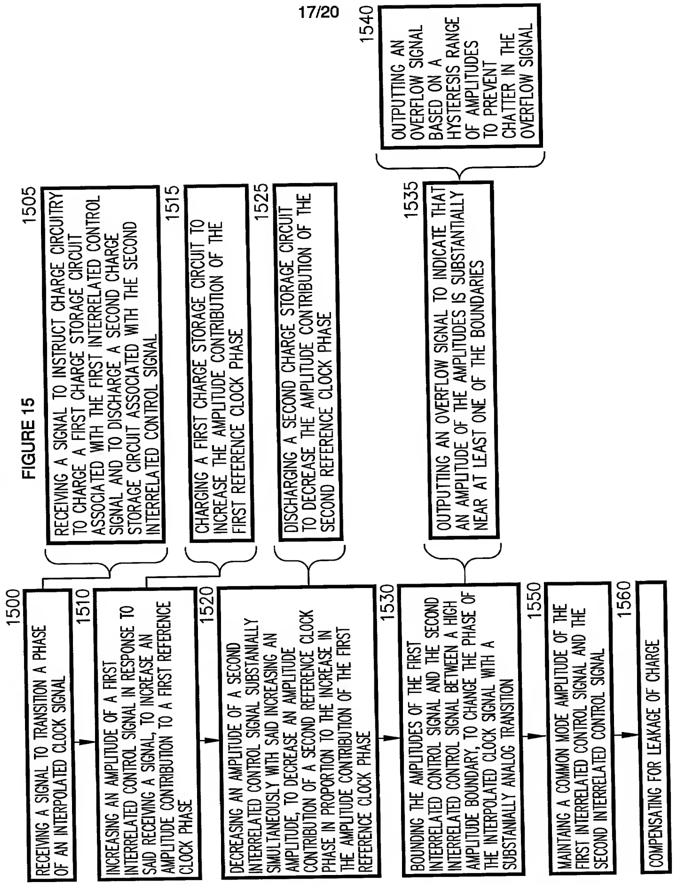
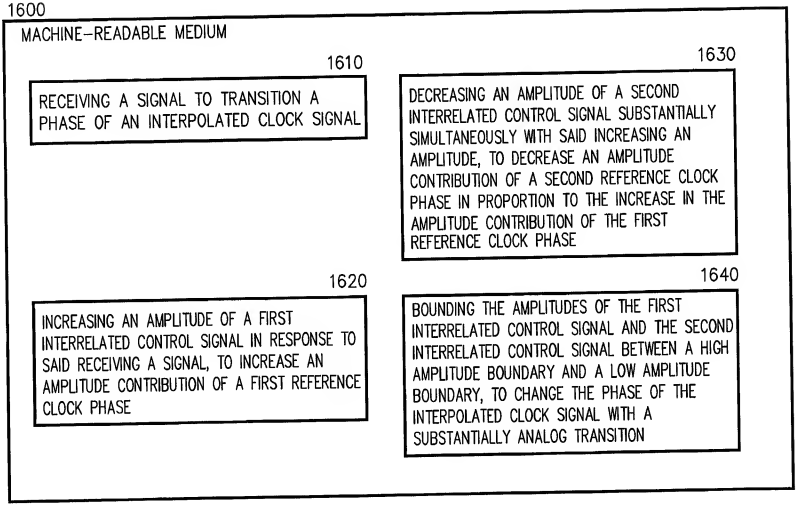


FIGURE 16



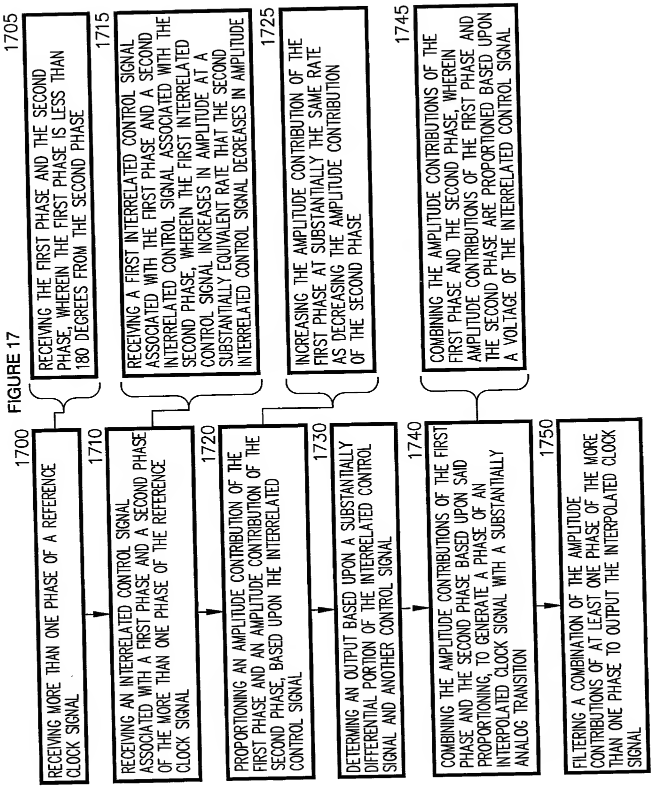


FIGURE 17
1700
RECEIVING MORE THAN ONE PHASE OF A REFERENCE CLOCK SIGNAL
1705
RECEIVING THE FIRST PHASE AND THE SECOND PHASE, WHEREIN THE FIRST PHASE IS LESS THAN 180 DEGREES FROM THE SECOND PHASE
1710
RECEIVING AN INTERRELATED CONTROL SIGNAL ASSOCIATED WITH A FIRST PHASE AND A SECOND PHASE OF THE MORE THAN ONE PHASE OF THE REFERENCE CLOCK SIGNAL
1715
RECEIVING A FIRST INTERRELATED CONTROL SIGNAL ASSOCIATED WITH THE FIRST PHASE AND A SECOND INTERRELATED CONTROL SIGNAL ASSOCIATED WITH THE SECOND PHASE, WHEREIN THE FIRST INTERRELATED CONTROL SIGNAL INCREASES IN AMPLITUDE AT A SUBSTANTIALLY EQUIVALENT RATE THAT THE SECOND INTERRELATED CONTROL SIGNAL DECREASES IN AMPLITUDE
1720
PROPORTIONING AN AMPLITUDE CONTRIBUTION OF THE FIRST PHASE AND AN AMPLITUDE CONTRIBUTION OF THE SECOND PHASE, BASED UPON THE INTERRELATED CONTROL SIGNAL
1725
INCREASING THE AMPLITUDE CONTRIBUTION OF THE FIRST PHASE AT SUBSTANTIALLY THE SAME RATE AS DECREASING THE AMPLITUDE CONTRIBUTION OF THE SECOND PHASE
1730
DETERMINING AN OUTPUT BASED UPON A SUBSTANTIALLY DIFFERENTIAL PORTION OF THE INTERRELATED CONTROL SIGNAL AND ANOTHER CONTROL SIGNAL
1740
COMBINING THE AMPLITUDE CONTRIBUTIONS OF THE FIRST PHASE AND THE SECOND PHASE BASED UPON SAID PROPORTIONING, TO GENERATE A PHASE OF AN INTERPOLATED CLOCK SIGNAL WITH A SUBSTANTIALLY ANALOG TRANSITION
1745
COMBINING THE AMPLITUDE CONTRIBUTIONS OF THE FIRST PHASE AND THE SECOND PHASE, WHEREIN AMPLITUDE CONTRIBUTIONS OF THE FIRST PHASE AND THE SECOND PHASE ARE PROPORTIONED BASED UPON A VOLTAGE OF THE INTERRELATED CONTROL SIGNAL
1750
FILTERING A COMBINATION OF THE AMPLITUDE CONTRIBUTIONS OF AT LEAST ONE PHASE OF THE MORE THAN ONE PHASE TO OUTPUT THE INTERPOLATED CLOCK SIGNAL

FIGURE 18